HARDWARE DEVICE FOR PROCESSING THE TASKS OF AN ALGORITHM IN PARALLEL

Abstract

A hardware device for processing the tasks of an algorithm of the type having a number of processes the execution of some of which depend on binary decisions has a plurality of task units (10, 12, 14), each of which are associated with a task defined as being either one process or one decision or one process together with a following decision. A task interconnection logic block (16) is connected to each task unit for communicating actions from a source task unit to a destination task unit. Each task unit includes a processor (18) for processing the steps of the associated task when a received action requests such a processing. A status manager (20) handles actions coming from other task units and builds actions to be sent to other task units